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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,631	07/20/2001	Steven C. Miller	062986.0201	1774

7590 03/11/2004

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	5

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No	Applicant(s)	
	09/910,631	MILLER ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16,21* is/are rejected.

7)☒ Claim(s) *8,17,20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Srbljiic et al US Patent 5,933,849.

In regards to claim 18, Srbljic discloses a computer system, comprising:

a main system memory operable to store system data in column 5 lines 61-65;

a remote memory operable to store copies of data from the main system memory for use by a remote device in figure 10 element 1003; and

a memory protocol operable to provide a copy of data to the remote memory from the main system memory, to automatically delete the copy from the remote memory after a period of time and to automatically update a status of the data at the main system memory upon expiration of the period of time without notification messaging between the main system memory and the remote memory in column 3 line 60 through column 4 line 14.

In regards to claim 21, Srbjlic discloses a system for managing data at an input/output (I/O) interface for a computer system, comprising:

a computer processable medium in column 5 lines 61-65; and

logic stored on the computer processable medium, the logic operable to provide a copy of data stored in a system memory to a remote memory, to automatically invalidate the copy in the remote memory after a predefined period of time, and to automatically update a status of the data in the system memory after the period of time in column 3 line 60 through column 4 line 14.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pawlowski et al. US PGPUB 2002/0029358 in view of Srbljic et al. US Patent 5,933,849.

In regards to claim 1, Pawlowski discloses a multiprocessor system, comprising:

a processing sub-system including a plurality of processors and a processor memory system in figure 2, P0-P3 and MEM0-MEM3 and caches associated with P0-P3;

a network operable to couple the processing sub-system to an input/output (I/O) sub-system in figure 2 element 210;

the I/O sub-system including a plurality of I/O interfaces each operable to couple a peripheral device to the multiprocessor system figure 2 elements IOP and IOD0 and 1;

the I/O interfaces each including a local memory operable to store a copy of data from the processor memory for use by a corresponding peripheral device in figure 2 cache located inside IOP; and

a directory for the processor memory system, the directory operable to identify the data as owned upon providing the copy to the I/O sub-system in figure 2 element DIR.

Pawlowski does not disclose the I/O interface invalidating a data copy at a first time event and the directory identifying data as unowned at a second time event. Srbljic discloses using a time to live parameter which is used to perform cache coherence without the need for network cache messaging in column 14 lines 6-35, Srbljic is concerned with minimizing network traffic in large scale multiprocessor systems, Pawlowski is and example of such system therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Srbljic's cache coherency policies in Pawlowski's architecture.

In regards to claim 2, Srbljic discloses the first and second time event occur at the same time by the specification of one time parameter in which both the source and destination act upon the expiration of said parameter as shown in column 3 line 60 through column 4 line 14.

In regards to claim 3, Srbljic discloses the first and second time event comprise expiration of a predefined period of time after an initiation event in column 14 lines 11-14.

In regards to claim 4, Pawlowski discloses the network is a scalable network in figure 2 QSD0-QSD3.

In regards to claim 5, Pawlowski discloses the scalable network comprises a plurality of routers in figure 2 QSA and QSD.

In regards to claim 6, Pawlowski discloses the processor memory system comprises a plurality of discrete processor memories in figure 2 caches associated with processors P0-P3.

In regards to claim 7, Pawlowski discloses the discrete processor memories are each dedicated to a processor in figure 2 caches associated with processors P0-P3.

In regards to claim 9, Pawlowski discloses a method for managing data in an input/output (I/O) interface for a multiprocessor system, comprising:

coupling a plurality of processors to a processor memory system in figure 2 P0-P3 coupled to associated caches and MEM0-MEM3 via element 204;

coupling a plurality of I/O interfaces to the processor memory system in figure 2 element IOD0 and IOD1 via 204;

coupling a peripheral device to each I/O interface figure 2 element 215;

storing a copy of data from the processor memory system in an I/O interface for use by a corresponding peripheral device figure 2 IOP cache;

Pawlowski does not disclose invalidating the copy in the I/O interface at a first time event, identifying the data as owned upon providing the copy to the I/O interface, and automatically identifying the data as unowned at a second time event. Srbljic discloses using a time to live parameter which is used to perform cache coherence without the need for network cache messaging in column 14 lines 6-35, Srbljic is concerned with minimizing network traffic in large scale multiprocessor systems, Pawlowski is and example of such system therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Srbljic's cache coherency policies in Pawlowski's architecture.

In regards to claim 10, Srbljic discloses the first and second time event occur at the same time by the specification of one time parameter in which both the source and destination act upon the expiration of said parameter as shown in column 3 line 60 through column 4 line 14.

In regards to claim 11, Srbljic discloses the first and second time event comprise expiration of a predefined period of time after an initiation event in column 14 lines 11-14.

In regards to claim 12, Srbljic discloses the initiation event comprises a time of initiation of a request for the copy of the data from the processor memory system in column 14 lines 11-14.

In regards to claim 13, Pawlowski discloses the network is a scalable network in figure 2 QSD0-QSD3.

In regards to claim 14, Pawlowski discloses the scalable network comprises a plurality of routers in figure 2 QSA and QSD.

In regards to claim 15, Pawlowski discloses the processor memory system comprises a plurality of discrete processor memories in figure 2 caches associated with processors P0-P3.

In regards to claim 16, Pawlowski discloses the discrete processor memories are each dedicated to a processor in figure 2 caches associated with processors P0-P3.

In regards to claim 19, Srbljic does not disclose the remote memory comprises a local cache of an input/output (I/O) interface for a peripheral device. Pawlowski discloses a system with a local cache for the I/O interface in figure 2 cache within IOP. Srbljic is concerned with minimizing network traffic in large scale multiprocessor systems, Pawlowski is and example of such system therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Srbljic's cache coherency policies in Pawlowski's architecture.

Allowable Subject Matter

Claims 8, 17, 20 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Major et al. US Patent 6,542,967, Lewis et al. US Patent 6,532,490, and Challenger et al. US Patent 6,457,103 all disclose using a time to live parameter to reduce network bandwidth.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan 3/8/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2188